AMENDMENTS TO THE SPECIFICATION

Please amend the specification as shown below.

Please amend the paragraph beginning on Page 9, line 13, with the following amended paragraph:

A buffer memory device [provide] provided with such a competition control circuit, however, has the disadvantage that sometimes continuous access of the memory is not possible.

Please amend the paragraph beginning on Page 33, line 14, with the following amended paragraph:

According to a 20th aspect of the present invention, there is provided an arithmetic device reconfigurable by outside control, comprising a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs and a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the computing units of [the] each stage in accordance with a control signal, the computing units arranged in the stages other than the computing units of the first stage each being supplied at the plurality of inputs with output data of the plurality of computing units of the previous stage, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

Please amend the paragraph beginning on Page 52, line 13, with the following amended paragraph:

Further, for example, the address generation device informs the control circuit of the end of the operation.

Please amend the paragraph beginning on Page 84, line 20, with the following amended paragraph:

Further, the arithmetic device is 10-I [is] outputs from the coefficient output terminals PE_C0O to PE_CkO the coefficient delayed by exactly the desired amount of delay by the C0FIFO18-0 to CkFIFO18-k as the coefficient outputs c0i to cki to the arithmetic devices 10-i + 1 of the next stage and outputs from the data output terminals PE_D0O to PE_DmO the data delayed by exactly the desired amount of delay by the D0FIFO19-0 to DmFIFO19-m as the data outputs d0i to dmi to the arithmetic device 10-i + 1 of the next stage.